REMARKS/ARGUMENTS

Applicant thanks Examiner Mai for the careful examination of the application and for clearly explaining the rejections. Applicant responds to the Office action as follows:

1. Claim 18 is amended to overcome the 112 rejection. As amended, the claim particularly points out and distinctly claims the regions of invention in claim 18 as the drift region, the intermediate-doped region, and the drain region.

2. The 103(a) rejection against claim 10 is improper.

   a. Both the Kwon reference and the Zhu reference lack at least one element in claim 10.

      As it is correctly pointed out in the Office action, the Kwon reference does not teach a field oxide structure spaced apart from the gate electrode region. Neither does the Zhu reference even though the Office action assumes otherwise.

      The mistake stems from Figure 1 in the Zhu reference. In drawings 1(a) and 1(b), the GATE feature lies over the OXIDE region, the N-Well region, the P-Body region and the N+ region. In both drawings, there is a gap between the GATE feature and the P-body region. Any person skilled in the art would recognize the LDMOS device in the Zhu reference refers to a Metal-Oxide-Semiconductor device and in order for such a device to function, there must be a layer of oxide between the MOS gate electrode and the semiconductor channel region – the P-Body region in this case. There could be two possible reasons why the oxide element is missing in the drawings in Zhu reference:

         1. It is a draftsman's error, or

         2. The gate oxide is so well known by persons in the art that the Authors left it out of the drawing without any concern of being misconstrued.

It is well known in the art that conventionally, the gate oxide is grown from the semiconductor material in the channel region. It is also well known in the art that during the gate oxide growth, a corresponding layer of oxide will grow on top of an existing oxide region. Therefore, it is reasonable to draw the gate conductor in Fig. 1(a) and 1(b), as lying over the oxide region but leaving a gap signifying the gate oxide on the channel region and the additional oxide grown on the existing oxide. Nevertheless, a layer of oxide must exist between the gate conductor (electrode) and the channel and there must be an additional growth of oxide between the gate conductor and the thick oxide to fill the gap in Figs. 1(a) and 1(b) lest the gate structure collapses.

b. The Kwon reference teaches away from having a gate electrode spaced apart from the oxide.

The Kwon teaches a thin gate insulator grown over the entire surface of transistor 10 extending on IGFET body 28 to thick insulator layer 26. A conductive gate 32 is then formed over the entire surface of transistor 10, and is then etched away to extend over IGFET body 28 on thin gate insulator 30 and onto thick insulator layer 26.[1] The Kwon reference specifically teaches a gate conductor formed over the thick insulator, not spaced apart from it as claimed in claim 10 of the current invention.

c. The references do not teach nor suggest combining the "spaced-apart" and there is no incentive for doing so.

Individually, there is no teaching the "spaced-apart" limitation and there is no suggestion to separate the gate conductor from the thick oxide. To implement such an element in either reference, there must be additional process steps of inserting a different material between the gate conductor and the thick oxide. Yet there is no incentive for doing so in the device as configured in the references.

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[1] See, U.S. Patent No. 5,406,110, col. 3, ll. 24-27.

In conclusion, because the references both lack the "spaced-apart" limitation, the Kwon reference specifically teaches away from this limitation and there is no teaching, suggestion, or incentive to combine this limitation, the 103 rejection is improper. Therefore, claim 10 is patentable over the references.

3. The 103(a) rejections against Claims 11-17 are not proper.

a. Claim 11 depends on patentable claim 10 with additional limitation that the drift region 14 comprising an N-type dopant.

b. Claim 12 depends on patentable claim 10 with additional limitation that the doping concentration of the intermediate-doped region being higher than that of the drift region.

c. Claim 13 depends on patentable claim 10 and further includes a drain region with higher doping concentration than in the intermediate-doped region.

d. Claim 14 depends on patentable claim 10 and further includes a buried layer adjacent to a portion of the body region.

e. Claim 15 depends on patentable claim 10 and further includes a LOCOS structure adjacent a portion of the drain region.

f. Claim 16 depends on patentable claim 10 and further includes a spacer structure adjacent a portion of the gate electrode.

g. Claim 17 depends on patentable claim 10 and further includes a drain contact to facilitate a flow of current through the device.

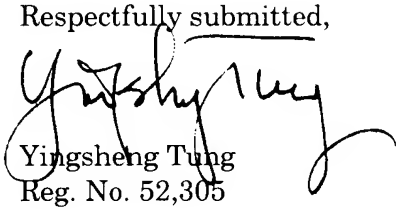
Claims 11-17 are patentable over the cited references.

4. The new claim 19 is fully supported by the original specification[2] and original drawing.[3] It distinguishes the cited references and therefore, is patentable.

[2] See, e.g., p. 12, 1st paragraph.
[3] See, Figure 5.

Applicant respectfully submits that the amended application is in allowable form and the claims are distinguishable over the cited references. Applicant respectfully requests further examination and consideration of this application.

Respectfully submitted,



Texas Instruments Incorporated
P. O. Box 655474 MS 3999
Dallas, TX 75265
(972) 917-5355

Yingsheng Tung
Reg. No. 52,305

In the Claims

1. (withdrawn)

2. (withdrawn)

3. (withdrawn)

4. (withdrawn)

5. (withdrawn)

6. (withdrawn)

7. (withdrawn)

8. (withdrawn)

9. (withdrawn)

10. (original) A semiconductor device, comprising:

a body region of a semiconductor substrate;

a drift region adjacent at least a portion of the body region, the drift region comprising a dopant;

a field oxide structure adjacent a portion of the drift region and a portion of a drain region, wherein the field oxide structure is located between a gate electrode region and the drain region and is spaced apart from the gate electrode region;

an intermediate-doped region adjacent a portion of the field oxide structure, the intermediate-doped region comprising dopant atoms accumulated proximate the field oxide structure;

a gate oxide adjacent a portion of the body region; and

a gate electrode adjacent a portion of the gate oxide.

11. (original) The semiconductor device of Claim 10, wherein the dopant comprises phosphorous.

12. (original) The semiconductor device of Claim 10, wherein the intermediate-doped region has a higher doping concentration than a doping concentration of the drift region.

13. (original) The semiconductor device of Claim 10, further comprising a drain implant at the drain region, the drain implant having a higher doping concentration than a doping concentration of the intermediate-doped region.

14. (original) The semiconductor device of Claim 10, further comprising a buried layer of the semiconductor substrate, wherein the buried layer is adjacent a portion of the body region.

15. (original) The semiconductor device of Claim 10, further comprising a local oxidation on silicon (LOCOS) isolation structure adjacent a portion of the drain region.

16. (original) The semiconductor device of Claim 10, further comprising a spacer structure adjacent a portion of the gate electrode.

17. (original) The semiconductor device of Claim 10, further comprising a drain contact at the drain region, the drain contact operable to facilitate a flow of electric current through the semiconductor device.

18. (currently amend) The semiconductor device of Claim 10, wherein ~~a relationship between a doping concentration of the semiconductor device and a lateral distance from he drift region is generally linear~~ the drift region has a first dopant concentration, the intermediate-doped region has a second dopant concentration, and the drain region has a third dopant concentration; and there exists a increment from the first doping concentration to the second doping concentration and a increment from the second doping concentration to the third dopant concentration; and the increments are approximately linear.

19. (new) The semiconductor device of Claim 18, wherein the difference between a peak doping concentration in the drift region and a peak doping concentration in the is approximately equal to the difference between the peak doping concentration in the intermediate-doped region and the peak doping concentration in the drain region.